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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/058,544	01/25/2002	Scott W. Mitchell	TI-32531	3761

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EXAMINER
TANG, MINH NHUT

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 08/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/058,544	MITCHELL ET AL.	
	Examiner	Art Unit	
	Minh N. Tang	2829	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election of species of Fig. 5 in Paper No. 3 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

It is noted that all claims are examined.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: references number "20" and "30" are not shown in Fig. 2. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The form and legal phraseology often used in patent claims, such as ***"means", "said", "comprising"*** should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

5. Claims 5, 12, and 15 are objected to because of the following informalities:

a/ in claims 5, 12, and 15, all in line 1, "and" should be deleted.

b/ in claim 11, lines 2-3, "said circuitry having said array of contact points" should be -- said array of contact points --.

c/ in claim 14, lines 1-4, "The method of manufacturing apparatus for simultaneously making electrical contact with an array of contact points on circuits having said array of contact points positioned according to a first :selected pattern comprising the steps of:" should be -- A method of manufacturing apparatus for simultaneously making electrical contact with an array of contact points on circuits, said array of contact points positioned according to a first selected pattern, comprising the steps of: --.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-16, 18, and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, the limitation "said support structure" (line 9, counted by hand) has not been recited previously; therefore this term is indefinite. For examination purposes, "said support structure" is interpreted as -- said support substrate --.

In claim 7, the limitation "at least two conductive probes of said multiplicity of having their ends adjacent each other at a single one of said multiplicity of locations" (lines 11-12, counted by hand) is unclear. For examination purposes, the limitation above is interpreted as -- at least two conductive probes of said multiplicity of conductive probes having their ends adjacent each other at a single one of said multiplicity of locations --.

In claim 11, the limitation "extending a multiplicity of first conductive probes through said multiplicity of apertures" (lines 10-11, counted by hand) is vague because it is unclear whether or not each conductive probe of the multiplicity of first conductive probes would extend through each corresponding aperture of the multiplicity of apertures. Additionally, it is not clear "a first end" and "a contact end" (line 11) refer to a first and contact ends of which device. Furthermore, it is also unclear "said conductive probes" (line 16, counted by hand) refers to which probes (i.e., first conductive probes or second conductive probe or both). For examination purposes, the limitations "extending a multiplicity of first conductive probes through said multiplicity of apertures such that a first end is at said back side and a contact end extends a selected distance beyond said working surface" and "positioning said multiplicity of apertures such that said contact ends of said conductive probes" are interpreted as -- extending each of first conductive probe of a multiplicity of first conductive probes through each aperture of

said multiplicity of apertures such that a first end of each first conductive probes is at said back side and a contact end of each first conductive probes extends a selected distance beyond said working surface" and "positioning said multiplicity of apertures such that said contact ends of said first conductive probes and said second conductive probe --, respectively.

In claim 14, it is unclear "said contact ends", "said conductive probes" (all in line 17, counted by hand) refer to contact ends of which probes. For examination purposes, "said contact ends", and "said conductive probes" are interpreted as -- said contact ends of said first conductive probes and said second conductive probe --, and -- said first conductive probes and said second conductive probe --, respectively.

In claims 18 and 19, the limitations "said first area", and "said second area" have not been recited previously; therefore these terms are indefinite. For examination purposes, "said first area" and "said second area" are interpreted as -- said area of a first size -- and -- said area of a second size --, respectively.

Claims 2-6, 8-10, 12-13, and 15-16 are rejected since they depend on rejected base claims.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Noda (U.S.P. 6,404,213).

As to claim 1, Noda discloses, in Figs. 17 and 20, apparatus (31) for simultaneously making electrical contact with an array of contact points (5) having a first selected pattern (i.e., constructed by contact points 5) on a circuit (semiconductor device), comprising: a support substrate (34) having a working surface (i.e., upper surface of substrate 34) and a back side (i.e., lower surface of substrate 34), said support substrate (34) defining a multiplicity of apertures (i.e., holes for inserting probes 21 or 21a in Fig. 20) extending from said backside (lower surface) through said substrate (34) and terminating at said working surface (upper surface) according to a second selected pattern corresponding to a mirror image of said first selected pattern; a multiplicity of conductive probes (21 or 21a in Fig. 20), said conductive probes (21a) extending from a first end (i.e., lower end of probe 21 or 21a) at said back side (lower surface) of said support substrate (34), through said apertures (i.e., holes) to a contact end (i.e., upper end of probe 21 or 21a) located a selected distance beyond said working surface (upper surface); at least one aperture (i.e., holes for inserting probes 21 or 21a) of said multiplicity of apertures including at least two conductive probes (22a, 23a, Fig. 20) extending there-through; a multiplicity of conductive pathways (i.e., body of each conductive probes 22a, 23a) extending from said first end (lower end) of said conductive probes (22a, 23a) to selected circuitry; and said conductive probes (22a, 23a) positioned through said support substrate (34) to make electrical contact with

contact points (5) on a circuit (semiconductor device) placed against said apparatus (31).

As to claim 2, Noda discloses in Fig. 17, said support substrate (34) comprises a planer insulating material.

As to claim 3, Noda discloses said contact points (5) are conductive bumps or balls (i.e., pads).

As to claim 4, Noda discloses in column 10, lines 30-35, and column 7, line 41 through column 8, line 15, said at least two conductive probes (22a, 23a) extending through said at least one aperture (i.e., hole) are connected one each to a voltage source line and a voltage sensing device.

As to claim 5, Noda discloses in Fig. 17, a third conductive probe (i.e., another probe(s) 21a adjacent the previous probe) connected to another voltage source.

As to claims 6 and 10, Noda discloses in column 10, line 30, said apparatus (31) is a probe card for testing integrated circuits.

As to claim 7, Noda discloses, in Figs. 17 and 20, an apparatus (31) for simultaneously making electrical contact with an array of contact points (5) positioned according to a first selected pattern (i.e., constructed by contact points 5) on a circuit (semiconductor device) comprising: an insulating support substrate (34) having a working surface (i.e., upper surface of substrate 34) and a back side (i.e., lower surface of substrate 34); a multiplicity of conductive probes (21 or 21a in Fig. 20), each of said conductive probes (21a) extending from a first end (i.e., lower end of probe 21 or 21a) at said backside (lower surface) of said substrate (34), through said substrate (34) to a

contact end (i.e., upper end of probe 21 or 21a), contact ends (upper end) of said multiplicity of conductive probes (21a) extending a selected distance beyond said working surface (upper surface) and terminating at a multiplicity of locations (i.e., locations for making connection with wiring 36 in Fig. 17) arranged according to a second selected pattern corresponding to a mirror image of said first selected pattern; at least two conductive probes (22a, 23a) of said multiplicity of conductive probes (21a) having their ends adjacent each other at a single one of said multiplicity of locations (see Fig. 20); and said contact ends (upper ends) of said conductive probes (22a, 23a) positioned through said support substrate (34) to make electrical contact with selected ones of said contact points (5) on a circuit placed against said apparatus (31).

As to claim 8, Noda discloses in Figs. 17 and 20, at least two of said multiplicity of locations include at least two of said conductive probes (21a).

As to claim 9, Noda discloses in Figs. 17 and 20, at least two of said multiplicity of locations include at least three of said conductive probes (21a).

As to claim 11, Noda discloses, in Figs. 17 and 20, a method of manufacturing apparatus (31) for simultaneously making electrical contact with an array of contact points (5) on circuitry (semiconductor device), said array of contact points (5) positioned according to a first selected pattern (i.e., constructed by contact points 5), comprising the steps of: providing a support substrate (34) having a working surface (i.e., upper surface of substrate 34) and a backside (i.e., lower surface of substrate 34); defining a multiplicity of apertures (i.e., holes for inserting probes 21 or 21a in Fig. 20) extending from said backside (lower surface) through said substrate (34) and terminating at said

working surface (upper surface) according to a second selected pattern, said second selected pattern corresponding to a mirror image of said first selected pattern; extending each of first conductive probe (22a) of a multiplicity of first conductive probes (also called 22a) through each aperture (hole) of said multiplicity of apertures (holes) such that a first end (i.e., lower end of probe 22a) of each first conductive probes (22a) is at said back side (lower surface) and a contact end (i.e., upper end of probe 22a) of each first conductive probes (22a) extends a selected distance beyond said working surface (upper surface); extending a second conductive probe (23a) having a first end (i.e., lower end of probe 23a) and a contact end (i.e., upper end of probe 23a) through at least one of said multiplicity of apertures (holes); and positioning said multiplicity of apertures (holes) such that said contact ends (upper ends) of said first conductive probes (22a) and said second conductive probe (23a) are aligned to make electrical contact with at least a portion of said array of contact points (5) of a circuit (semiconductor device) placed against said apparatus (31).

As to claims 12 and 15, Noda discloses in Figs. 17 and 20, placing circuitry (semiconductor device) having an array of contact points (5) against said apparatus (31) and testing said circuitry (semiconductor device).

As to claims 13 and 16, Noda discloses in column 10, lines 30-35, and column 7, line 41 through column 8, line 15, a selected probe (22a) of said multiplicity of first conductive probes (22a) is for supplying a selected voltage and said second conductive probe (23a) adjacent said selected probe (22a) is for sensing a voltage.

As to claim 14, Noda discloses, in Figs. 17 and 29, a method of manufacturing apparatus (31) for simultaneously making electrical contact with an array of contact points (5) on circuits (semiconductor devices), said array of contact points (5) positioned according to a first selected pattern (i.e., constructed by contact points 5), comprising the steps of: providing a support substrate (34) having a backside (i.e., lower surface of substrate 34) and a working surface (i.e., upper surface of substrate 34); extending a multiplicity of first conductive probes (22a) through said support substrate (34), each of said first conductive probes (22a) extending from a first end (i.e., lower end of probe 22a) at said backside (lower surface) of said substrate (34), through said substrate (34) to a contact end (i.e., upper end), said contact ends (upper ends) of said conductive probes (22a) extending a selected distance beyond said working surface (upper surface) and terminating at a multiplicity of locations (i.e., locations for making connection with wiring 36 in Fig. 17) according to a second selected pattern corresponding to a mirror image of said first selected pattern; extending at least one second conductive probe (23a) having a first end (i.e., lower end of probe 23a) and a contact end (i.e., upper end of probe 23a) through said substrate (34), said contact end (upper end) of said at least one second conductive probe (23a) terminating adjacent the contact end (upper end) of one of said multiplicity of first conductive probes (22a); and positioning said contact ends (upper ends) of said first conductive probes (22a) and said second conductive probe (23a) such that said first conductive probes (22a) and said second conductive probe (23a) are aligned so as to make electrical contact with said

array of contact points (5) of a circuit (semiconductor device) placed against said apparatus (31).

As to claim 17, Noda discloses, in Figs. 17 and 20, an apparatus (31) for contacting a target test point (5) having an area of a first size on an integrated circuit comprising: a substrate (34); and at least two electrically isolated probes (22a, 23a) supported by said substrate (34) located within an area of a second size for simultaneously contacting said target test point (5).

As to claim 18, Noda discloses in Figs. 17 and 20, said area of a first size is smaller than said area of a second size.

As to claim 19, Noda discloses in Figs. 17 and 20, said area of a first size is greater than said area of a second size.

As to claim 20, Noda discloses in column 10, lines 30-35, and column 7, line 41 through column 8, line 15, one of said at least two electrically isolated probes (22a, 23a) is for applying a voltage and a second one of said probes (22a, 23a) is for sensing a voltage.

As to claim 21, Noda discloses, in Figs. 17 and 20, a process for providing a voltage at a target test point (5) on an integrated circuit comprising the steps of: contacting said target test point (5) with first and second probes (22a, 23a); applying a voltage to said target test point (5) through said first probe (22a); sensing a voltage at said target test point (5) through said second probe (23a); and adjusting said voltage applied through said first probe (22a) until a selected voltage is sensed by said second probe (23a).

As to claim 22, Noda discloses in Figs. 17 and 20, contacting said target test point (5) with a third probe (any other probe 21a), applying another voltage to said target test point (5) through said third probe (any other probe 21a) and adjusting said voltage applied through said third probe (any other probe 21a) until another selected voltage is sensed by said second probe (23a).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Tarzwell 5,982,187 Resilient Connector Having A Tubular Spring.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh N. Tang whose telephone number is (703) 305-1652. The examiner can normally be reached on M-F (6:30-4:00) first Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mrs. Cuneo, Kamand can be reached on (703) 308-1233. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-3431.

Minh Tang
August 11, 2003